REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 22-25 are presently active in this case, Claim 21 canceled and Claims 22 and 23 amended and Claim 25 added by way of the present amendment.

In the February 21, 2002 Official Action Claims 21-24 were rejected under 35 U.S.C. §112, second paragraph, and Claims 21-24 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 3,760,384 to Krolikowski et al. the Board Decision reversed this rejection under § 112, second paragraph, and affirmed the rejection under § 102(b).First, Applicants wish to thank Examiner Pyonin and Supervisory Patent Examiner (SPE) Elms for the March 12, 2002 personal interview (prior to the appeal in this case) at which time the outstanding issues in this case were discussed. During the personal interview, new Claim 25 was discussed in relation to the cited reference to Krolikowski et al. While no agreement was reached, the Examiners indicated that Claim 25 would overcome the rejection under 35 U.S.C. §112, second paragraph, and may overcome the rejection based on Krolikowski et al, but further search would be required.

With regard to the rejection under 35 U.S.C. §112, second paragraph, while this rejection was reversed by the Board, Applicants note that Claim 21 has now been canceled and replaced with new Claim 25. In addition, as discussed in the March 12th personal interview, new Claim 25 includes the phrase "intellectual property functional circuit." As disclosed in Applicant's specification at page 2, lines 22 - page 3, line 2, the term "intellectual property" refers to a circuit component comprised of a plurality of circuit elements and which performs a certain function. Thus, the term "intellectual property" is clearly defined in Applicant's specification as originally filed. Therefore, 35 U.S.C. §112, second paragraph, no

further rejection is anticipated. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work with the Examiner in a joint effort to derive mutually satisfactory claim language.

Turning now to the merits, in order to expedite issuance of a patent in this case, Claim 21 has been canceled and Claim 25 has been added to clarify the patentable features of the present invention over the cited reference to Krolikowski et al. Specifically, new Claim 21 recites a method of manufacturing an electronic circuit having a plurality of separate intellectual property functional circuits on a single semiconductor chip. The method includes storing a library of layout patterns including layout patterns of the intellectual property functional circuits, storing a diagram of the electronic circuit, and generating a mask pattern for each of the intellectual property functional circuits based on the stored library. Also recited is the step of transferring each of the mask patterns to a predetermined position on the semiconductor chip such that the intellectual property functional circuits are adjacent to each other and not overlapping.

In contrast, Krolikowski et al discloses a method of fabricating an FET memory chip. The method uses separate masks to define and form the different regions of the FET devices. The method uses a conventional masking system wherein a first mask is used to form a first part of the FET device, and subsequent masks are placed over the area of the first mask to form other parts of the FET devices. For example, as described in column 11, lines 23-45, a mask A is used to form the source and drain regions of the FET, and masks B, C, and D are used to form other areas of the FET such as contacting holes and metallization patterns. Because each mask defines a portion of the same FET, masks must be carefully aligned to maintain a desired spacing. As discussed in the March 12th interview, the alignment masks of Figure 9 are used to ensure that each mask is placed precisely where the previous mask was

placed on the semiconductor chip. Thus, Krolikowski et al does not disclose transferring each of the mask patterns to a predetermined position on the semiconductor chip such that the intellectual property functional circuits are adjacent to each other and not overlapping as now recited in Claim 25.

Therefore, new Claim 25 patentably defines over the cited reference. Moreover, as Claims 22-24 depend from Claim 25, these claims also patentably define over the cited reference.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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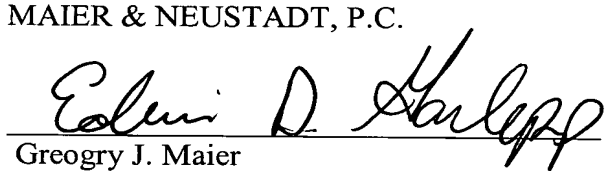

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